MODEL 1623-15
WORD GENERATOR

Serial No._____

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0967

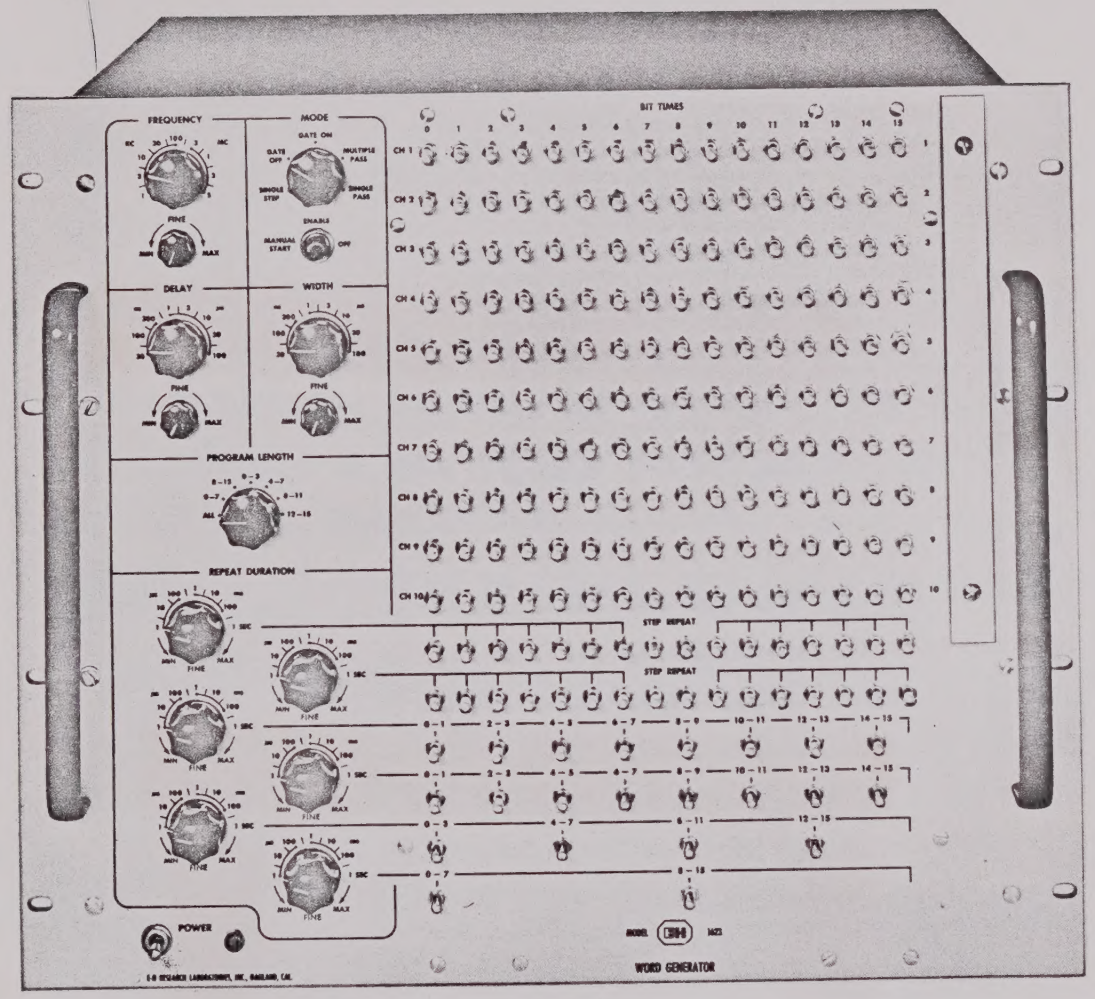


Fig.1-1 Model 1623 WORD GENERATOR

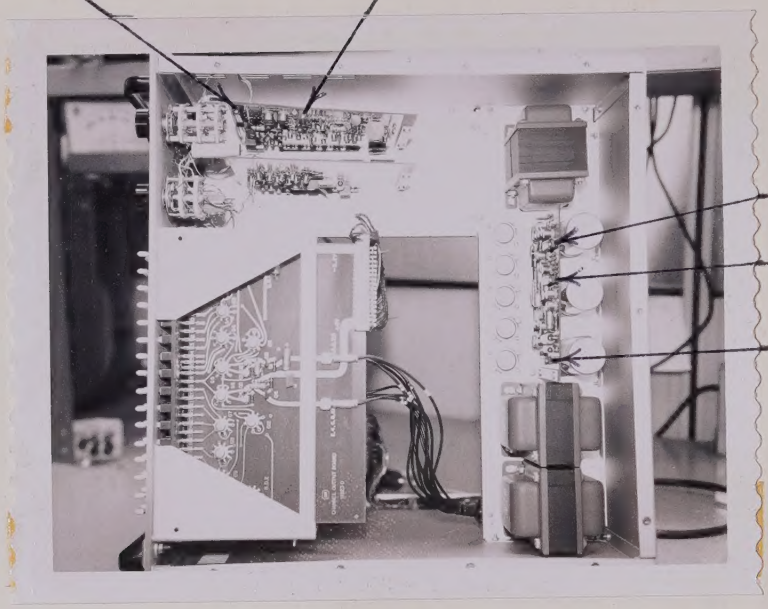


FIG. #1 VIEW FROM TOP

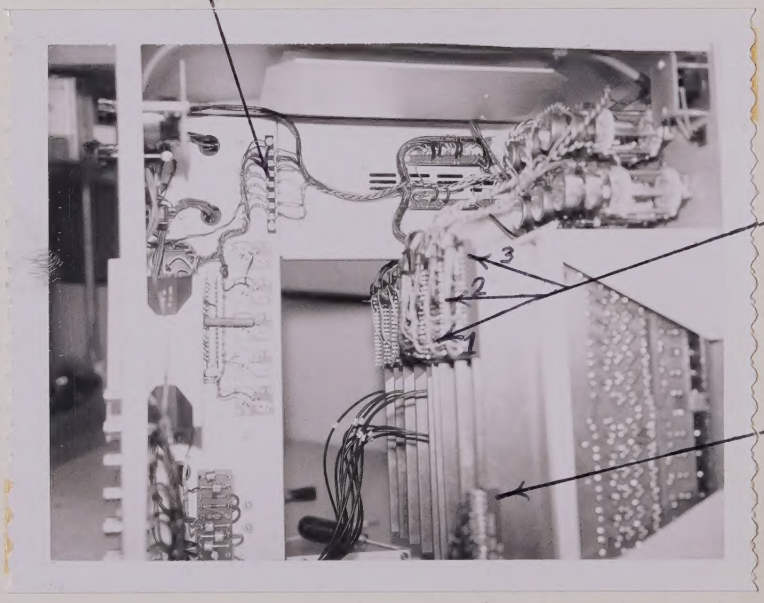


FIG. #2 VIEW FROM BOTTOM

CALIBRATION OF E. H. 1623 WORD GENERATOR

REMOVE UNIT FROM RACK, TAKE OFF TOP & BOTTOM COVERS. ALSO REMOVE & CLEAN FILTER.

SET THE FOLLOWING 1623 FRONT PANEL CONTROLS AS INDICATED:

1) FREQUENCY TO MAX., FINE CONTROL TO MAX.
2) MODE SWITCH TO GATE OFF.
3) DELAY TO MIN., FINE CONTROL TO MIN.
4) WIDTH TO MIN., FINE CONTROL TO MIN.
5) ALL REPEAT DURATION CONTROLS TO MIN
6) ALL STEP REPEAT SWITCHES TO OFF
7) ALL BIT TIME SWITCHES TO OFF
8) ENABLE SWITCH TO OFF.
9) PROGRAM LENGTH TO ALL

1) POWER SUPPLIES:

   A) CHECK AT THE INDICATED TEST POINTS ($\pm$ 2%) AND ADJUST IF NECESSARY THE +15V, +8V AND -5.2V POWER SUPPLIES.

   B) CHECK ($\pm$ 2%) THE -15V AND -2V POWER SUPPLIES.

   C) CHECK ALL POWER SUPPLIES FOR RIPPLE (2MV P/P MAX)

2) FREQUENCY: SET COUNTER TO MEASURE FREQUENCY AND MONITOR THE SYNC OUTPUT J 102 TERMINATED IN 50Ω AT COUNTER.

   A) MOVE ENABLE SWITCH TO MANUAL START AND ADJUST R79 ON THE CONTROL BOARD FOR 10.3 MEGAHERTZ (E.H. SPEC). IT MAY TAKE SEVERAL SECONDS FOR THE OSCILLATOR TO STABILIZE AFTER ADJUSTMENT OF R79.

   B) CHECK ALL FREQUENCY RANGES FOR OVERLAP.

3) SYNC OUTPUT:
RESET: FREQUENCY COURSE CONTROL TO MAXIMUM AND THE FINE CONTROL TO MINIMUM.
MONITOR THE SYNC OUTPUT WITH THE SAMPLING OSCILLOSCOPE. (SET SCOPE TO 200 MV/DIV, 10 NS/CM SWEEP AND USE A X 2 ATTENUATOR).

   A) ADJUST R42 ON THE CONTROL BOARD FOR A 72 NS PULSE WIDTH AT THE 50% POINTS. (E.H. SPEC).

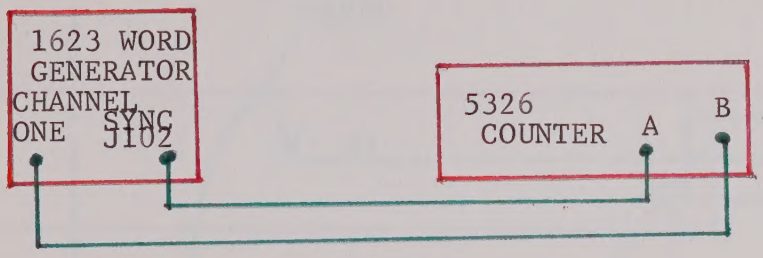
   B) CHECK FOR RISE AND FALL TIMES OF LESS THAN 5NS, AND AMPLITUDE OF GREATER THAN 1.25V.

4) WIDTH:
RESET: CHANNEL ONE BIT TIME ZERO TO ON POSITION. CONNECT CHANNEL ONE OUTPUT TO COUNTER TERMINATED IN 50Ω. SET COUNTER TO MEASURE TIME INTERVAL.

   A) CHECK FOR MIN. WIDTH.

B) CHECH FOR RANGE OVERLAP OF WIDTH CONTROL (REMEMBER TO DECREASE FREQ AS WIDTH IS INCREASE.

5) DELAY:
RESET: WIDTH CONTROLS TO MIN.
CHANNEL ONE ALL BIT TIMES TO ON, CONNECT EQUIPMENT AS SHOWN:



A) CHECK MIN DELAY SETTING:

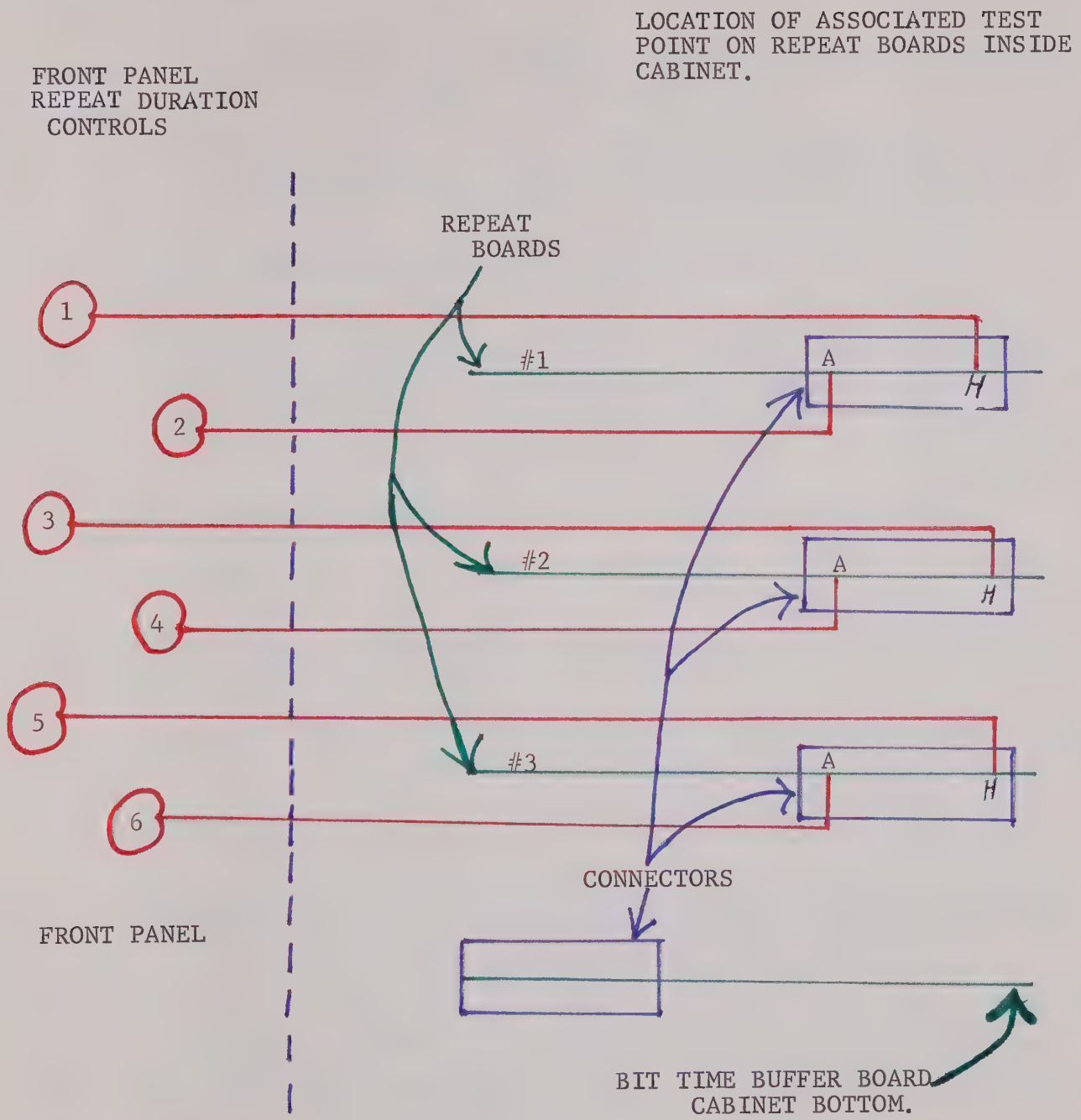
Delay time is referred to the SYNC pulse, which precedes the actual output signal by approximately 60 NS, plus the indicated front panel delay time.

MINIMUM MEASURED DELAY TIME WILL BE 90 NS OR LESS.
MAXIMUM DELAY ON THE LOWEST RANGE SHOULD BE GREATER THAN THE MINIMUM MEASURED DELAY PLUS 70 NS.

B) CHECK ALL DELAY RANGES FOR OVERLAP DECREASING FREQUENCY AS DELAY IS INCREASED.

6) REPEAT DURATION:
RESET: FREQUENCY TO MAX, FINE CONTROL TO MID RANGE. DELAY CONTROLS TO MIN.

A) CHECK ALL REPEAT DURATION CONTROLS FOR PROPER TIMING AND RANGE OVERLAP BY MEASURING THE WIDTH OF THE ASSOCIATED TIMING PULSE INDICATED BELOW. (REFER TO PICTURE FOR LOCATION OF BOARDS INSIDE CABINET.).



7) CHANNEL OUTPUTS RESET CONTROLS:
   1) REPEAT DURATION CONTROLS TO MIN.
   2) REPEAT DURATION SWITCHES TO OFF.
   3) ALL CHANNEL BIT TIMES TO ON.
      A) CHECK THAT EACH CHANNEL OUTPUT INCLUDES ALL 16 BIT TIMES.

B) USE SAMPLING OSCILLOSCOPE AND CHECK THAT ON EACH CHANNEL OUTPUT THE PULSE RISE AND FALL TIMES ARE LESS THAN 15NS AND THE AMPLITUDE IS AT LEAST 2.5V.

C) MONITOR EACH OF THE BIT TIME OUTPUTS ON THE SAMPLING OSCILLOSCOPE AND CHECK FOR PULSE RISE AND FALL TIMES OF 15NS OR LESS AND PULSE AMPLITUDES OF AT LEASE 1.0V.

8) MONITOR THE CHANNEL ONE OUTPUT ON THE 454 SCOPE AND CHECK FOR PROPER OPERATION OF THE PROGRAM LENGTH SWITCH.

Program length selector: Determines program length, and selects bits included in program of word output. At ALL position the basic word output has 16 bits. In the 0-7 and 8-15 positions the word output has 8 bits; the first 8 or the second 8 respectively. Similarly, for the 0-3, 4-7, 8-11, and 12-15 positions, the program length is 4 bits.

9) CHECK FOR PROPER OPERATION OT THE MODE SWITCH USING THE 454 SCOPE AND DATA PULSE 101.

Clock Modes:

Single Step: Manual control for output of one bit at a time. Single Step output is controlled by 3-position switch (manual start-enable-off) below mode selector.

Gate Off: Clock free-runs at selected frequency when manual switch starts program. Clock stops when manual start switch is reset to off.

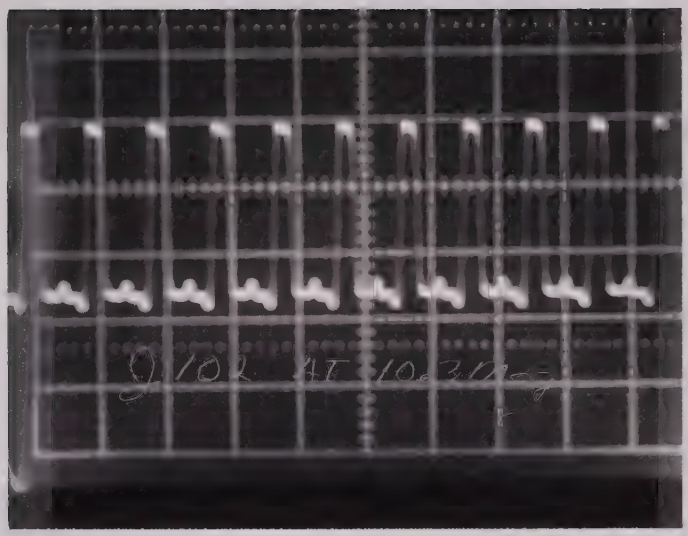
Gate On: Clock free-runs only for duration of gate signal at Gate in connector.

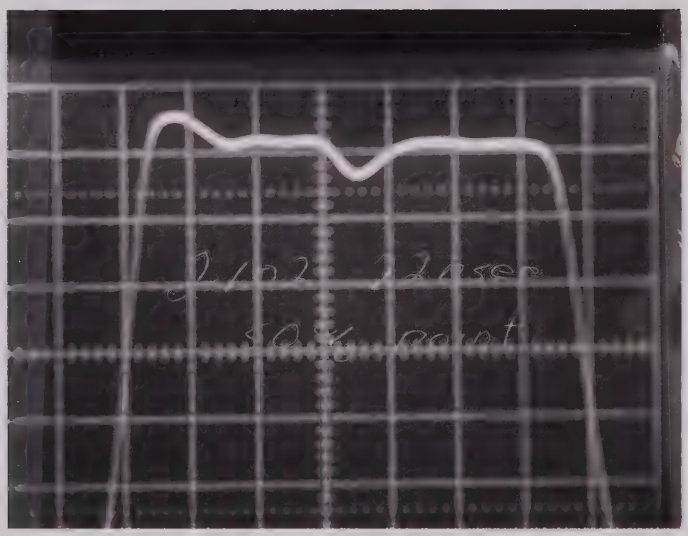
Multiple Pass: External signal enables internal clock to generate an integral number of complete programs, as a function of the gate signal duration. At the end of the gate signal, the clock completes a program and stops. Clock is synchronous with gate.

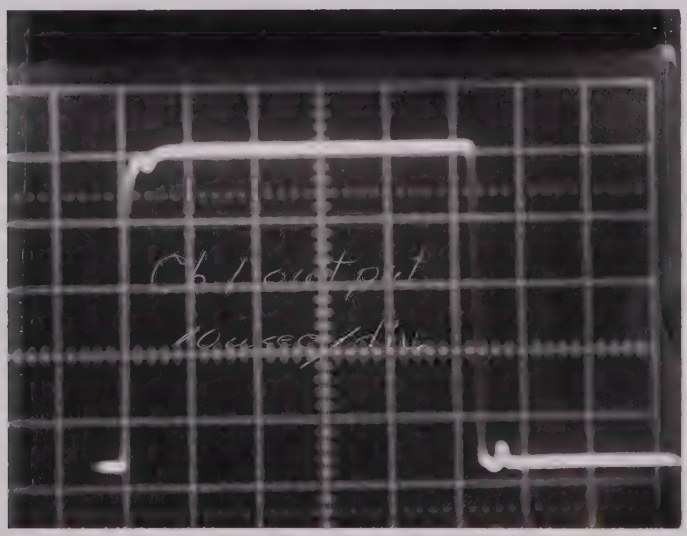
Single Pass: External gate signal or manual start switch enables clock for one (1) program only, clock is synchronous with gate.

10) CHECK FOR PROPER OPERATION OF GROUND "1" GROUND "0" SWITCH USING 454 SCOPE + DATA PULSE 101.

GRD "0", GRD "1" TOGGLE SWITCH (REAR PANEL):
Provides selection of gate input signal level. At GRD '0' position ground potential is logical 0; voltage excursions away from ground (Logical 1) initiates program output. At GRD '1' position, ground potential is logical 1, and voltage excursions to ground initiates program output.







1221 TIMING UNITS

1. Check Pin 4 +15 V and Pin 1 −15 V power supplies (± .5 V)
Use adjustment to bring both supplies in spec.
This adjustment is not critical nor absolutely necessary (per EH). Check ripple. (20 mv)

2. Using a realtime oscilloscope, check the following on each channel. Use positive or negative pulses (10 ns or >) to trigger the 1221, and trigger the scope accordingly.

Suggest 556, 2-14H's to see max # (balanced) of channels at one time when doing steps b, c, d, and e

a) Minimum input trigger voltage, (< 1.5 V)
Input impedance is 50 ohms.

b) Output amplitude (> 5 V into 50 ohms)

c) Trigger output 1 amplitude (2 V from 2 V reference level into 50 ohms)

d) Pulse width min./max. continuously variable.
(< 20 ns. to > 1 ms.)

e) Trigger width min./max. continuously variable.
(< 20 ns to > 1 ms)

f) Delay from leading edge of input pulse to leading edge of output pulse. (fixed at approx 20 ns).

2. g) Input trigger frequency (DC to 10 MegHz.)
   h) Duty factor (>70 %)

3. With a sampling oscilloscope check the following on each channel.

   a) Output pulse rise and fall time (< 8 ns)
   Output to sampler through 10 x attenuator.
   Trigger terminated in 50 ohms.
   Width course set at minimum, fine at 2 o'clock position.

   b) Trigger pulse rise and fall time (< 8 ns)
   Output terminated in 50 ohms.
   Trigger to sampler through 5 X attenuator.
   Width same as 3a.

MODEL 153-5
DATA RATE MODIFICATION

CHANGES

A. Specifications

1. Rise time <3ns
2. V noise < ± 200 micro volts peak to peak - 95% probability.
3. Accuracy < 2% of signal ± noise
4. Transient response < 1% peak to peak - 8ns - D.C.
5. Vt response < 2% from 6ns - D.C.
6. V zero vs frequency shift < 1mv
7. Programming time < 5 micro seconds for 1% full scale.
8. Data rate 100KHz Max. to single shot.

B. Schematic

1. Input delay line removed.
2. Vt out and trigger in connector removed from front panel and add to rear panel
3. Add C1A 10pf (311-051) in parallel with C1 on sampler card.
4. Change clip line on sampler card to 48" length.
5. Change R32 to 365Ω 1% (617-046) on sampler card.
6. Change R34 to 562Ω (617-045) 1% on sample card.
7. Remove C3 on trigger card.
8. Change C8 to .001 mfd (311-010) on trigger card.
9. Change C1 to 400pf (311-026) on trigger card.

081468DR/pl

DISCRIMINATOR

1 The back panel is layed out as follows:

J1 — SYSTEM STROBE

J2–J5 — 4 ENABLE INPUTS

J6 — SIGNAL INPUT

J7 — DATA OUTPUT

2 Board A11 A14 A17

Delay gen	GPIC #1	GPIC #2	REFERENCE SUPPLY	DISCRIMINATOR	BUFFER AMP	DISCRIMINATOR	BUFFER AMP

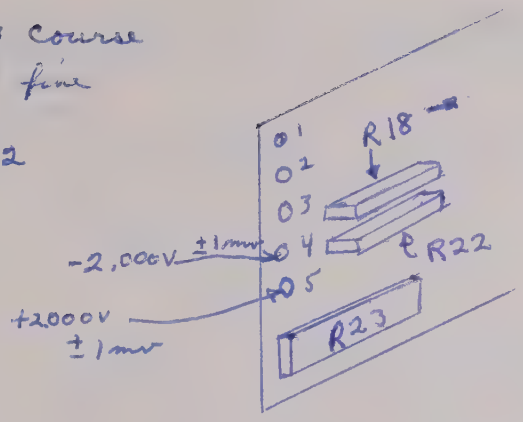
3 The discriminator unit is done last.

4 The gain of the operational amplifier will be reset when the unit is attached to the strobing voltmeter.

A14 Board

- 2V { R23 Course
R18 fine

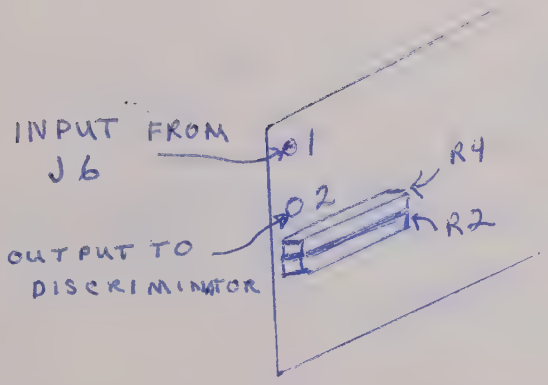
+2V R22



pictures

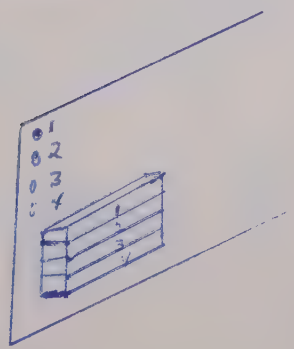
A17

R4 ZERO
R2 GAIN



A11

R1 - R4 control flash rate of fail lights (20ms nom.)

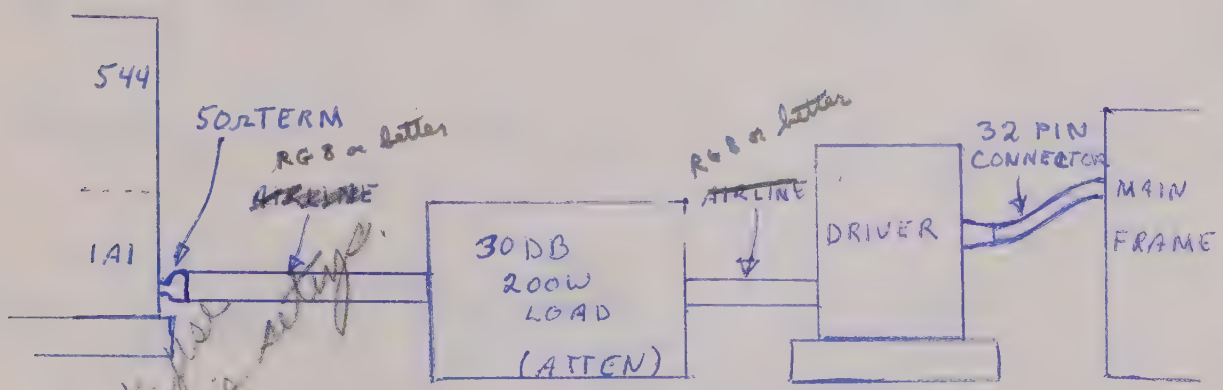


DRIVERS

1. Use the Fluke 853A and Tek. 544/1A1/1S1 or equivelent.
2. Follow the calibration procedure with these exceptions.

Note!!

C1) With no signal and no trigger, set the +10 volt adjustment to bring both +10V and -10V supplies in specification. (per EH)



~~CAUTION~~: This is a rigid ~~system~~ do not force, bend, or ~~twist~~. Adjust the height of the ~~oscilloscope~~ and driver to allow insertion of the airlines.

C2) Using the above setup, set the Vcc adjustment for 1.6V. (51V through 30DB terminated in 50 ohms)

Note!!

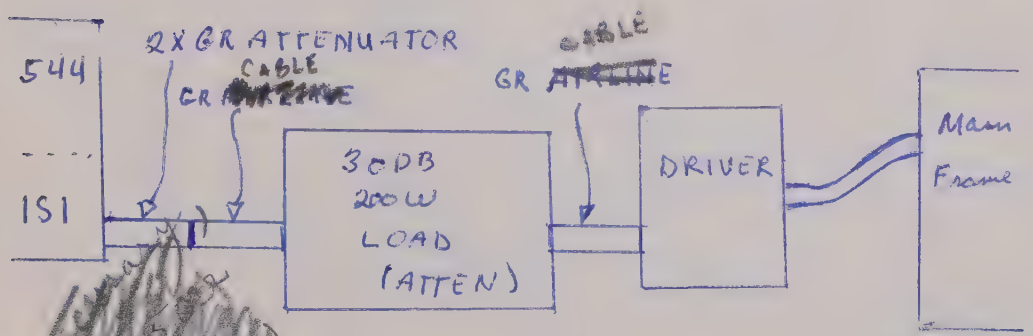
Check scope gain at .5V/cm, set if more than 2% against standard amplitude calibrator. (Check .2V/cm position and note any error for use when D/A cards are adjusted)

C2 cont) If the D/A card is installed this setting is only a preliminary adjustment, otherwise it is a final adjustment.

DRIVER VOLTS	TERMINATED OUTPUT OF 30DB LOAD
52 V	1.64V
51 V	1.61 V
50 V	1.58 V

C4. The extender is only needed if D/A cards are installed in the driver. Set the 15 V adjustment to bring both +15 V and -15 V in specification.

f Use the following setup for waveshape adjustments.



1S1 — .1V/cm ; 100ns/cm

DRIVER — SET FOR .5 V amplitude

TRIG INPUT — 10ns or faster ; 1.5V to 3V amplitude with clean rise and fall times.
See NOTE on pag 4-3 of the Manual.

f Make adjustments at 50 or 100 ns/cm then check front edge for aberations (20 ns/cm) and linearity of leading edge. Check rise and fall times.

Check operation of front panel controls.
The D/A cards will be done with the assembled system.

When the units are finished and installed in the rack the following system checks and adjustments are made.

1 Connect the oscilloscope, discriminator, and strobing voltmeter together and trigger the units from the generator through the 1221 timing units.

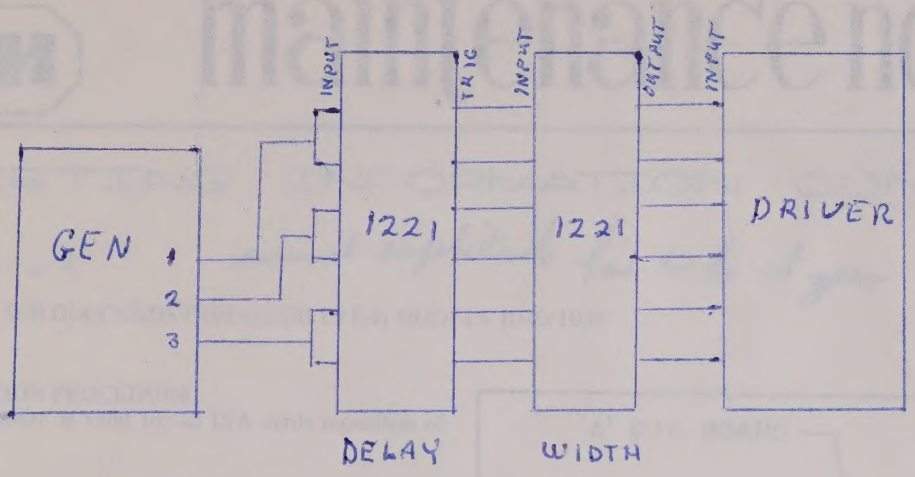
2 The discriminator loop gain must be reset to compensate for the loading effect of the discriminator on the strobing voltmeter. The scope reading of the voltage at V(t) will be approximately 8% lower than the true voltage at the input to the sampling voltmeter.

3 Monitor the voltage at the input of the sampler and reset the gain of the operational amplifier to obtain the correct front panel indication on the discriminator.

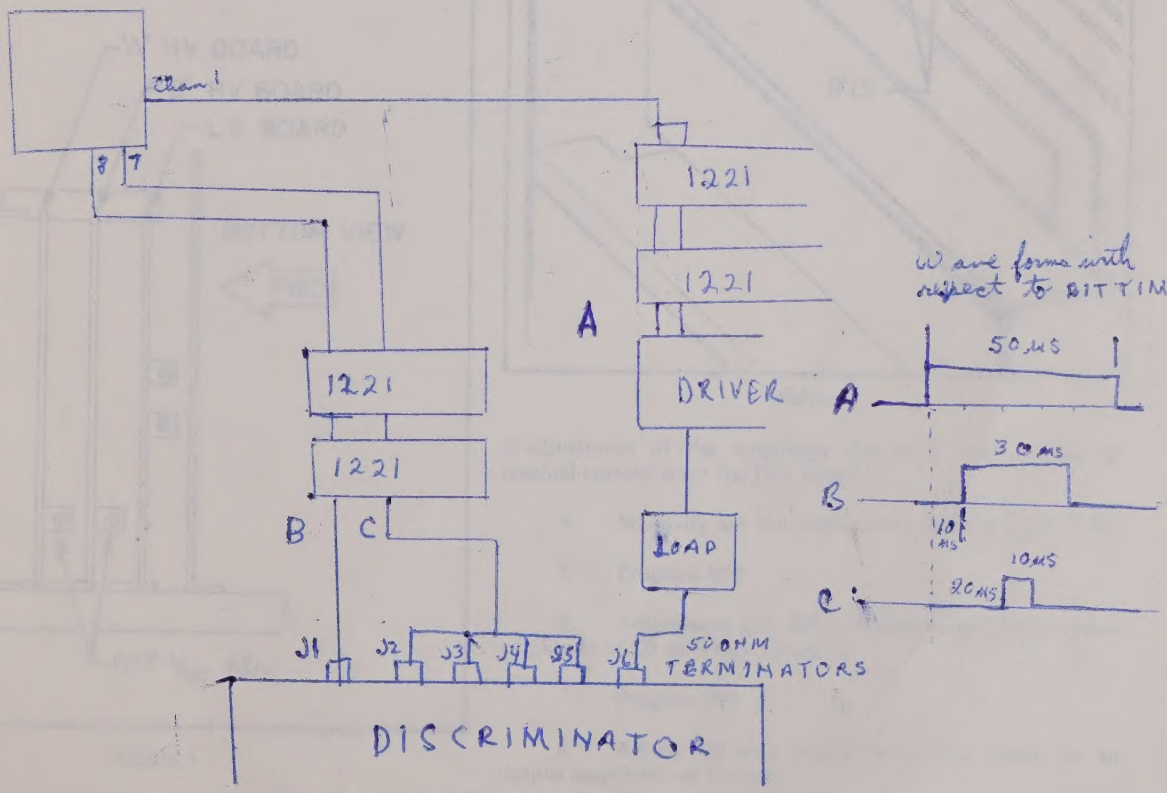
4 Adjust the D/A cards in the appropriate drivers.

5 Make checks for system jitter and noise.

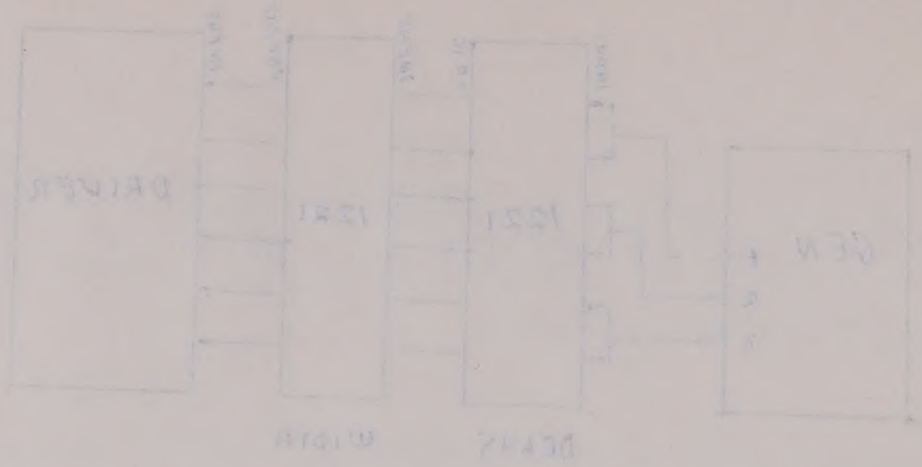
~~[illegible] at the output of sampler~~ when the sampler is loaded by the discriminator.

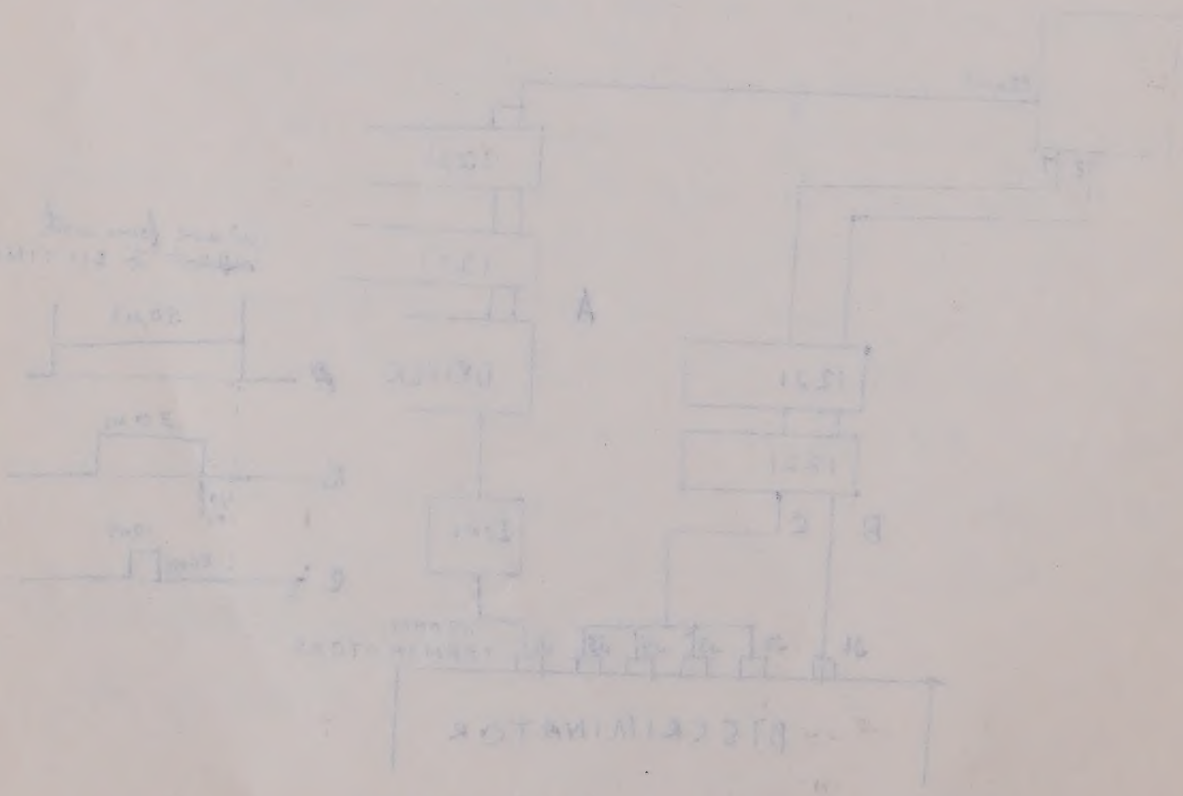


SET UP FOR SYSTEM CHECK OF DRIVERS AND ADJUSTMENT OF D/A CARDS IN THE DRIVERS.



SET UP FOR D/A CARDS




A
B
C

maintenance notes

MARKETING INFORMATION CONTROL

file code: 9-03-A

_8 manual amplitude has to be at zero

October 1968

Subject: MODEL 930 D/A CARDS INSTALLED IN E-H MODELS 1030/1033

Test: CALIBRATION PROCEDURE
(Note: This procedure is valid for all D/A cards regardless of logic.)

Purpose:
To enable the field calibration of 1030/33's not having 930 D/A cards installed at the factory. (Note: This procedure is valid for all D/A cards regardless of logic.)

Details of Procedure:

1. With the cards installed, manually set the amplitude to maximum. (full CW)

2. Program 000

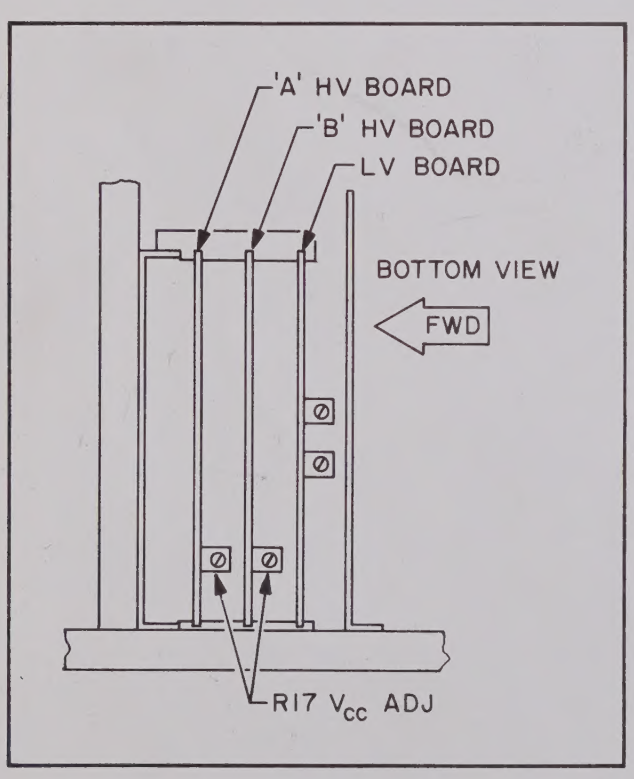


Figure 1

3. With the bottom cover removed, adjust the high voltage supply for an output amplitude of 52 volts, using R17 (see Figure 1). (Installing the D/A board necessitates the re-adjustment of the amplitude due to a small amount of residual current from the D/A board.)

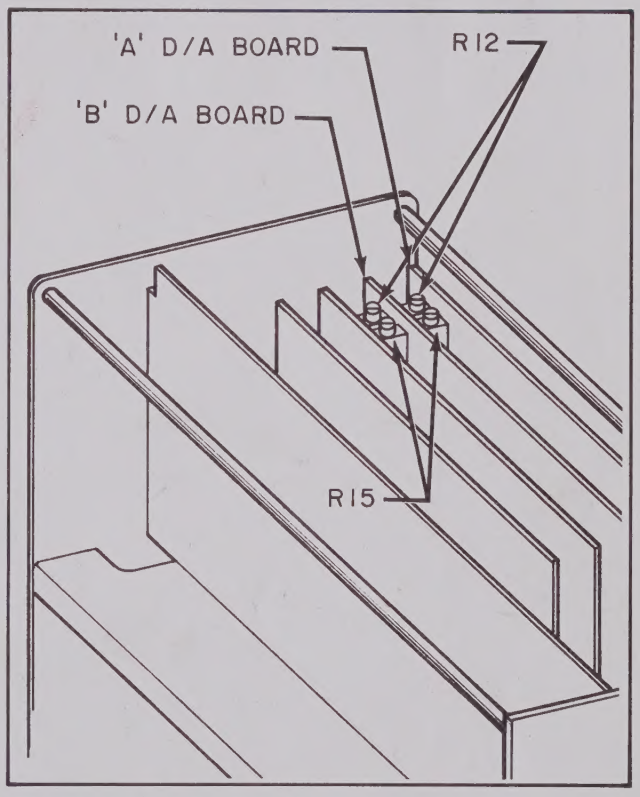


Figure 2

4. Manually set the amplitude to 0 volts (full CCW).

5. Program 400

6. Adjust zero pot, R12, on D/A board for an output amplitude of 20 volts (see Figure 2).

7. Program 999

8. Adjust full scale pot, R15 on D/A board, for an output amplitude of 50 volts.

9. Due to the interaction of the three adjustments, steps 3 thru 8 must be repeated until all digital settings produce an output voltage within 2% of full scale.

$$\frac{1.6}{51} = \frac{x}{20}$$

20
1.6
12.0
20 6 2
51 32.6 0
6 2 7

140
102
380

.627
51 32.0.0
306
140
102
380
35

$\frac{20}{51}$ $\frac{x}{16}$